QP CODE: 18103826

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Reg No : .....

Name : .....

B.Sc.DEGREE(CBCS)EXAMINATION, DECEMBER 2018

First Semester

B.Sc Computer Science Model III

Complementary Course - EL1CMT06 - ELECTRONICS - FUNDAMENTALS OF DIGITAL SYSTEMS

2018 Admission only

46142D55

Maximum Marks: 80 **Time: 3 Hours**

Part A

Answer any **ten** questions.

Each question carries **2** marks.

1. (a) Determine the value of each digit in 939. (b) How high can you count with 4 bits?
2. Conver the decimal pairs -46 and 25 to binary and add using the 2's complement form.
3. State the rules for hexadecimal addition citing suitable examples.
4. Find the binary and hexadecial equivalent of 14768.
5. Implement the truth table and the logic circuit for the expression X=A'BC+AB'C'
6. Implement the expression ABC+DE with NAND logic.
7. Determine the truth table for the following standard POS expression (A+B+C)(A+B'+C)(A+B'+C') (A'+B+C')(A'+B'+C).
8. Design a 4X1 MUX.
9. Explain the operation of a gated SR latch
10. What is meant by present and next state?
11. Why are shift register considered basic memory devices?
12. How a shift register counter differs from a basic shift register?

(10×2=20)

Part B

Answer any **six** questions.

Each question carries **5** marks.

13. Perform the indicated operations. (a) 1101+1011 (b) 1100-1001 (c) 1110x1101 (d) 1001÷11.

14. Describe the functional differences between a NOR gate and a negative AND gate. Do they both have the same truth table?

15. Establish NOR gate as a Uiversal logic element

16. Realize the Basic gates using NAND and NOR gates.

17. Discuss commutative and associative laws of addition and multiplication in boolean algebrae.

18. Convert the expression AB'C+(AB)'+ABC'D to standard SOP form.

19. Develop a timing diagram and combinational logic circuit for the function X(=A(B+C))'

20. Compare a latch and a flip flop.

21. Design an asynchronous mod-12 counter

(6×5=30)

Part C

Answer any **two** questions.

Each question carries **15** marks.

22. Give an account of alphanumeric codes. (a) ASCII (b) EBCDIC and ©Parity Codes.

23. Using Boolean algebrae techniques simplify the following expressions and implement using logic gates of both before and after simplification (a) AB+A(B+C)+B(B+C) (b) (AB+AC)'+A'B'C (c) AB'C(BD+CDE)+AC'

24. Design a four bit magnitude comparator which checks for equality greater than and less than conditions.

25. With neat diagram and waveform explain a synchronous (a) decade counter (a) mod 12 counter

(2×15=30)